Please enter the following amendments:

In the Claims:

1. (Original) A method for programming a memory cell having two bits positioned between two current conductors comprising:

toggling the logic state of the two bits; and

toggling the logic state of one of the two bits.

2. (Original) The method of programming a memory cell as claimed in claim 1 further comprising reading the two bits to obtain stored information and comparing the stored information to program information to be written prior to toggling the two bits.

3. (Currently Amended) A method for programming a memory cell having two bits positioned between two current conductors comprising:

toggling a logic state of a first of the two bits; and

toggling ~~the~~ a logic state of a second of the two bits ~~each bit~~ ~~separately~~ independently of toggling the logic state of the first of the two bits.

4. (Original) The method of programming a memory cell as claimed in claim 3 further comprising reading the two bits to obtain stored information and comparing the stored information to program information to be written prior to toggling each of the two bits.

5. (Currently Amended) A method for programming a memory cell having two bits positioned between first and second current conductors comprising:

deciding on one of or both of the steps comprising:

applying current to each of the conductors, thereby ~~setting~~ toggling the logic state of the two bits; and

applying a smaller current to each of the conductors, thereby ~~setting~~ toggling the logic state of only one of the bits.

6. (Original) The method of programming a memory cell as claimed in claim 5 further comprising reading the two bits to obtain stored information and comparing the stored information to the information to be written prior to setting the logic state of the two bits.

7. (Currently Amended) A method for programming a memory cell having first and second bits positioned between first and second current conductors, comprising:

deciding on one of the steps comprising:

programming the first and second bits by applying first and second currents to the first and second current conductors, respectively;

programming the first bit to switch a state of the first bit by applying the second current to the second conductor and a third current

to the first conductor, the third current being less in magnitude than the first current; and

programming the second bit to switch a state of the second bit by applying the first current to the first conductor and a fourth current to the second conductor, the fourth current being less in magnitude than the second current.

8. (Original) The method of programming a memory cell as claimed in claim 7 further comprising reading the two bits to obtain stored information and comparing the stored information to the information to be written prior to programming.

9. (Currently Amended) A method for programming a memory cell having first and second bits positioned between first and second current conductors comprising:

programming the first bit to toggle its present bit state by applying one of a positive current in both the first and second current conductors ~~and~~ or a negative current in both the first and second current conductors; and

programming the second bit to toggle its present bit state by applying a positive current in one of the first and second current conductors and a negative current in the other of the first and second current conductors.

10. (Original) The method of programming a memory cell as claimed in claim 9 further comprising reading the two bits to obtain stored information and comparing the stored information to program information to be written prior to programming each of the first and second bits.

11. (Original) A method of switching a magnetoresistive memory device having a magnetoresistive memory element adjacent to a first conductor and a second conductor wherein the magnetoresistive memory element comprises first and second bits, the first bit including a first magnetic region and a second magnetic region separated by a first tunneling barrier, the second bit including a third magnetic region and a fourth magnetic region separated by a second tunneling barrier, at least one of the first and second magnetic regions and at least one of the third and fourth magnetic regions include N ferromagnetic material layers that are anti-ferromagnetically coupled, where N is an integer equal to at least two, and where each layer has a magnetic moment adjusted to provide a writing mode, and also each of the first, second, third and fourth magnetic regions has a magnetic moment vector oriented in a preferred direction at a time t0, the method comprising:

turning on a first current flow through the first conductor at a time t1;

turning on a second current flow through the second conductor at a time t2;

turning off the first current flow through the first conductor at a time t3; and

turning off the second current flow through the second conductor at a time t4 so that one of the magnetic moment vectors for each of the first and second bits is oriented in a direction different from the initial preferred direction at the time t0.

12. (Original) The method of switching a magnetoresistive memory device as claimed in claim 11 wherein the magnetic moment of each layer of the N layers is set to provide a direct write mode at an operating current such that the current in each of the first and second conductors is pulsed with a same polarity to write a state and the current in each of the first and second conductors is pulsed with an opposite polarity to reverse the state.

13. (Original) The method of switching a magnetoresistive memory device as claimed in claim 12 wherein the time t3 is approximately equal to t4 so that the magnetoresistive memory device operates in the direct write mode at the operating current.

14. (Original) The method of switching a magnetoresistive memory device as claimed in claim 13 wherein the time t1 is approximately equal to t2 so that the magnetoresistive memory device operates in the direct write mode at the operating current.

15. (Original) The method of switching a magnetoresistive memory device as claimed in claim 11 wherein the magnetic moment of each layer of the N layers is set to provide a toggle write mode at an operating current such that the current in each of the first and second conductors is pulsed with a same polarity to write a state and the current in each of the first and second conductors is pulsed with the same polarity to reverse the state.

16. (Original) The method of switching a magnetoresistive memory device as claimed in claim 15 including in addition steps of reading the magnetoresistive memory device to obtain stored information and comparing the stored information to program information to be written prior to the step of turning on the first current flow.